CLAIMS

1. A method for adapting to specific needs an integrated circuit comprising a stack of insulating layers, each layer being associated with a determined metallization level, metal areas of the last metallization level forming electric contacts of the integrated circuit, comprising the steps of:

(a) forming pairs of metal regions of the penultimate metallization level having a facing edge and connected to components of the integrated circuit;

(b) depositing an insulating layer;

(c) etching according to the specific needs the insulating layer to expose the facing edges of the metal regions of determined pairs; and

(d) forming metal portions of the last metallization level which cover the facing edges of the metal regions of all pairs and which contact the metal regions of the determined pairs.

2. The method of claim 1, wherein step (d) comprises depositing a metal layer of the last metallization level, and delimiting in the metal layer said metal portions.

3. The method of claim 2, wherein the metal areas are delimited in the metal layer simultaneously with the metal portions.

4. The method of claim 3, further comprising:
depositing a passivation layer; and
etching openings exposing the metal areas.

5. The method of claim 1, wherein the etching of the insulating layer is a direct etching by an electron beam.

6. The method of claim 1, wherein the metal portions are metal connection balls.

7. An integrated circuit adapted to specific needs, comprising a stack of insulating layers, each layer being associated with a determined metallization level, metal

areas of the last metallization level forming electric contacts of the integrated circuit, comprising:

pairs of metal regions of the penultimate metallization level having a facing edge and connected to components of the integrated circuit;

insulating portions covering the edges of the metal regions of determined pairs according to the specific needs; and

metal portions of the last metallization level which cover the facing edges of the metal regions of all pairs and which connect the metal regions of the pairs other than the determined pairs.

8. The integrated circuit of claim 7, further comprising a passivation layer covering the metal portions.